06/19/00

"Express Mail" mailing label number EJ541080044US
Date of Deposit 6-16-00
I hereby certify that this application is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Commissioner of Patents and Trademarks Washington, D. C. 20231.
MaryEllen Dorish
(Printed name of person mailing paper or fee)
MaryEllen Dorish
(Signature of person mailing paper or fee)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

Sailesh Chittipeddi

CASE 79

TITLE A Process For Manufacturing An Integrated Circuit Including A Dual-Damascene Structure And A Capacitor

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

NEW APPLICATION UNDER 37 CFR § 1.53(b)

Enclosed are the following papers relating to the above-named application for patent:

Specification
7 Informal Sheets of drawing(s)
2 Assignment(s) with Cover Sheet
Declaration and Power of Attorney

CLAIMS AS FILED				
	NO. FILED	NO. EXTRA	RATE	CALCULATIONS
Total Claims	22 - 20 =	2	x $18 =	$36
Independent Claims	3 - 3 =	0	x $78 =	$0
Multiple Dependent Claims, if applicable			+ $260 =	$0
Basic Fee				$690
			TOTAL FEE	$726

Please file the application and charge **Lucent Technologies Deposit Account No. 12-2325** the amount of $726, to cover the filing fee. Duplicate copies of this letter are enclosed. In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Deposit Account No. 12-2325** as required to correct the error.

The Assistant Commissioner for Patents is hereby authorized to treat any concurrent or future reply, requiring a petition for extension of time under 37 CFR § 1.136 for its timely submission, as incorporating a petition for extension of time for the appropriate length of time if not submitted with the reply.

Please address all correspondence to **Docket Administrator (Room 3C-512), Lucent Technologies Inc., 600 Mountain Avenue, P.O. Box 636, Murray Hill, New Jersey 07974-0636.** However, telephone calls should be made to me at 610-712-3766.

Respectfully,

Anthony Grillo
Reg. No. 36535
Attorney for Applicant(s)

Date: 6/16/00

Lucent Technologies Inc.
600 Mountain Avenue (Room 3C-512)
P.O. Box 636
Murray Hill, New Jersey 07974-0636

A PROCESS FOR MANUFACTURING AN INTEGRATED CIRCUIT INCLUDING A DUAL-DAMASCENE STRUCTURE AND A CAPACITOR

Field of the Invention

The present invention relates generally to integrated circuits and, more particularly, to a process for forming dual damascene structures and capacitors in an integrated circuit.

Background of the Invention

Interdigitized or finger capacitors are being used more in integrated circuits as the height of metal lines in the integrated circuits become greater than the space between the metal lines. This occurs because device dimensions are decreasing which results in a corresponding decrease in distance between metal lines. Interdigitized or finger capacitors employ sidewall capacitance, the capacitance produced between adjacent metal lines to form a capacitor.

One example of a finger capacitor is shown in U.S. Patent No. 6.037,621 entitled ON CHIP CAPACITOR STRUCTURE and issued to Wilson. This patent is incorporated herein by reference. The concept of using sidewall capacitance to form capacitors is also discussed in a recent paper entitled Fractal Capacitors, H. Samavati, et al., 1998 ISSCC, Session 16, TD: Advanced Radio-Frequency Circuits, Paper FP 16.6, 256-57, which is incorporated herein by reference. The paper points out that sidewall or fringing capacitance yields a higher capacitance per unit area than conventional parallel plate capacitors as the distance between the plates decreases.

In addition to device dimension decreases, there has been trend to use dual damascene structures instead of single damascene structures. Single damascene is an interconnection fabrication process for integrated circuits in which grooves are formed in an insulating layer and filled with a conductive material to form interconnects. Dual damascene is a multi-level interconnection process in which, in addition to forming the grooves of single damascene, conductive contact (or via) openings are also formed in the

insulating layer. A conductive material is formed in the grooves and conductive contact (or via) openings. The inventor has recognized the need to combine these trends to provide a sidewall capacitor in an integrated circuit also including a dual damascene structure.

Summary of the Invention

The present invention is directed to a process for forming a dual damascene structure and a capacitor. The process includes forming a stack including insulating layers and a stop layer. The stack is patterned so that the openings used to form the sidewall capacitors may be formed when the vias or grooves of the dual damascene structure are formed. In this way, the process for manufacturing the sidewall capacitors may be integrated with the dual damascene process without adding additional mask or etching steps.

It is to be understood that both the foregoing general description and the following detailed description are exemplary, but are not restrictive, of the invention.

Brief Description of the Drawing

The invention is best understood from the following detailed description when read in connection with the accompanying drawing. It is emphasized that, according to common practice in the semiconductor industry, the various features of the drawing are not to scale. On the contrary, the dimensions of the various features are arbitrarily expanded or reduced for clarity. Included in the drawing are the following figures:

Fig. 1 is a flowchart diagram illustrating the process for manufacturing an integrated circuit according to an illustrative embodiment of the present invention;

Figs. 2-7 are schematic diagrams of an integrated circuit during successive stages of manufacture using the process of Fig. 1.

Fig. 8 is a top view of a partially fabricated integrated circuit including a finger capacitor and a dial damascene structure manufactured according to the process of Fig. 1;

Fig. 9 is a flowchart diagram illustrating the process for manufacturing an integrated circuit according to another illustrative embodiment of the present invention; and

Figs. 10-15 are schematic diagrams of an integrated circuit during successive stages of manufacture using the process of Fig. 9.

Detailed Description of the Invention

The illustrative embodiment of the present invention is directed to a process for forming a dual damascene structure. The process includes forming a stack including insulating layers and a stop layer where two masks are formed above the stack. One of the masks is used to form via or contact openings in the insulating layers and to form openings for a capacitor. The second mask is used to form grooves for interconnections in the insulating layers. By forming the openings for the capacitors when the grooves and vias for the dual damascene structure are formed, the number of processing steps and movement of the partially fabricated integrated circuit between systems may be reduced.

Referring now to the drawing, wherein like reference numerals refer to like elements throughout, Fig. 1 is a flow chart diagram illustrating an exemplary embodiment of the present invention. Figs. 2-7 are schematic diagrams illustrating the successive stages of manufacture of an integrated circuit according to the flow chart shown in Fig. 1.

At step 10, a first insulating layer 105 is formed on a substrate 100. The first insulating layer 105 is, for example, a dielectric such as a high-density deposited silicon oxide (e.g., SiO_2). Alternatively, the first insulating layer may be a borophosphosilicate glass, a phosphosilicate glass, a glass formed from phosphorous and/or boron-doped tetraethyl orthosilicate, spin-on glass, xerogels, aerogels, or other low

dielectric constant films such as a polymer, fluorinated oxide and hydrogen silsesquioxane. Further, the insulating layer may include multiple layers where at least one layer is a low dielectric constant material formed between other layers that may have a higher dielectric constant.

The substrate 100 is, for example, a semiconductor such as silicon or compound semiconductor such as GaAs or SiGe. Alternatively, the substrate 100 may be an intermediate layer in an integrated circuit such as a dielectric, conductor, or other material. In addition, the upper surface 101 of the substrate 100 may not be planar. In this case, the first insulating layer 105 may be planarized using, for example, chemical mechanical polishing (CMP) as is well known.

At step 15, an etch stop layer 110 is formed above or in direct contact with the first insulating layer 105. In an alternative embodiment, one or more layers may be formed between the etch stop layer 110 and the first insulating layer 105. The material for the etch stop layer may be selected to be more etch resistant than the second insulating layer 115 for a selected etchant. In other words, the etch stop layer 110 etches at a slower rate than the second insulating layer 105 when exposed to a selected etchant. For example, the etch stop layer may be TiN where the second insulating is SiO_2. Further, the etch stop layer may be Ta/TaN, Si_3N_4, a silicon-rich oxide, or a multi-layered $Si0_2$ dielectric.

At step 20, a second insulating layer 115 is formed above or in direct contact with the etch stop layer 115. The second layer 115 may be formed using the same materials and processes used to form the first insulating layer 105. At step 25, a first patterned mask 120 is formed above or on the insulating layer 115. The first patterned mask 120 includes openings that correspond to the via or contact openings 125 (hereinafter referred to as "openings") to provide interconnections between different levels in the integrated circuit. In addition, the first patterned mask 120 includes openings that correspond to the openings 127 for a capacitor (hereinafter referred to as the "capacitor openings"). The reticle 90 has a pattern so that capacitor openings 127 may be formed when openings 125 are formed.

At step 30, openings 125 and the capacitor openings 127 are opened in the first insulating layer 105, the etch stop layer 110, and the second insulating layer 115. The openings and the capacitor openings may be opened using conventional etching techniques or a combination of techniques to etch through at least the three different layers. Alternatively, step 30 may etch only the second insulating 115. In this case, at step 40, the exposed portion of the etch stop layer 110 and the corresponding portion of the first insulating 105 below the exposed portion would be etched to complete the capacitor openings 127 and the openings 125 when the groove is etched. The capacitor openings 127 may be formed in the same metallization level and not above or below each other

Illustratively, the openings are formed by: 1) applying a layer of resist material (the first patterned mask) on the second insulating layer 115; 2) exposing the resist material to an energy source which passes through a reticle; 3) removing areas of resist to form the pattern in the resist; and 4) etching the openings 125 and capacitor openings 127. The energy source may be an e-beam, light source, or other suitable energy source.

Subsequently, at step 35, a second patterned mask 130 is formed above or on the first patterned mask 120. Illustratively, the second patterned mask 130 is formed by: 1) applying a layer of resist material in the openings 125 and 127 on the first patterned mask 120; 2) exposing the resist material to an energy source which passes through a reticle 95; and 3) removing areas of resist to form the pattern in the resist. The energy source may be an e-beam, light source, or other suitable energy source.

The second patterned mask 130 includes openings for forming the grooves above the openings 125. The patterned mask 130 does not have corresponding openings for the capacitor openings 127 because the etching for these openings has already been completed. If the capacitor openings had not already been completed in the prior step as described above, then at step 35, openings would have been formed in the second patterned mask so that the capacitor's openings could be completed by subsequent processing.

At step 40, the second insulating layer 115 is patterned to form grooves 135 corresponding to the conductive runners and capacitor to be formed. The second insulating layer 115 may be patterned using conventional etching techniques. During etching, the etch stop layer 110 is used to define the endpoint for this etching process. The openings are contained or at least partially contained within the borders 136, 138 of the grooves 135. Then, at step 45, the remaining portions of the mask layers 120, 130 are stripped using well-known techniques and the partially completed integrated circuit is cleaned at step 47 using conventional processes.

At step 50, a conductive layer 145 is blanket deposited above the second insulating layer 115 and in the openings, grooves, and capacitor openings 127. Then, the portions of the conductive layer outside the capacitor openings 127 and the grooves 135 and on or above the second insulating layer are removed to complete the interconnect. This may be accomplished using a conventional chemical mechanical polishing process. The conductive layer 145 is a conducting material such as tungsten, aluminum, copper, nickel, polysilicon, or other conducting material suitable for use as a conductor and as is known to those skilled in this art.

By using this process a capacitor 170 is formed when the dual damascene structures 175 are formed. As a result, finger capacitors may be incorporated into the process for forming dual damascene structures without using additional process steps such as lithography processes and etching. In this way, increased costs for manufacturing an integrated circuit including finger capacitors may be avoided.

In an alternative embodiment, one of more layers, may be formed prior to the deposition of the conductive layer 145. An exemplary barrier layer 147 is shown in Fig. 7. These layers may be barrier layers preventing the migration of moisture and contaminants between the conductive layer and the surrounding layers.

For example, if the conductive layer 145 is copper, a barrier layer 147 including layers of Ta and TaN may be deposited on the second insulating layer 120 and in the openings and grooves prior to the deposition of the conductive layer. Where the conductive layer 145 includes Al, a barrier layer 147 including layers of (1) Ti and TiN or (2) Ti and TiN and Ti may be used. Other materials for the barrier layer include WSi,

TiW, Ta, TaN, Ti, TiN, Cr, Cu, Au, WN, TaSiN, or WSiN. The barrier layer 147 may also function as an adhesion layer and/or a nucleation layer for the subsequently formed conductive layer. In addition, a capping layer, such as Si_3N_4, TaN, TiN, or TiW may be formed on the upper surface of the conductive layer.

Figure 8 is a top view of an illustrative finger capacitor and a dual damascene structure formed using the above illustrative embodiment. The finger capacitor 170 includes a first plate 171 and a second plate 172. The interconnection of the capacitor with other portions of the integrated circuit has been omitted for clarity. One skilled in the art would be able to integrate the capacitor in an integrated circuit as necessary to compete the circuitry to be designed.

Subsequently, the integrated circuit is completed by adding, if necessary, additional metal levels that may including interconnects formed using the process above and conventional processes to complete an integrated circuit. The integrated circuit also includes transistors and other components necessary for a particular integrated circuit design. The processes for manufacturing an integrated circuit including these structures are described in 1-3 Wolf, Silicon Processing for the VLSI Era, (1986), which is incorporated herein by reference.

Figures 9-15 illustrate another alternative embodiment of the present invention. Fig. 9 is a flow chart diagram and Figs. 10-15 are schematic diagrams illustrating the successive stages of manufacture of an integrated circuit according to the flow chart shown in Fig. 9.

At step 210, a first insulating layer 305 is formed on a substrate 300. The first insulating layer 305 I is a material as described above with regard to the first insulating layer 105. The substrate 300 is a material as described above with regard to the substrate 100. In addition, the upper surface 301 of the substrate 300 may not be planar. In this case, the first insulating layer 305 may be planarized using, for example, chemical mechanical polishing (CMP) as is well known.

At step 215, an etch stop layer 310 is formed above or in direct contact with the first insulating layer 305. In an alternative embodiment, one or more layers may

be formed between the etch stop layer 310 and the first insulating layer 305. The etch stop layer 310 is a material such as the material described above with regard to the first etch stop layer 110.

At step 220, a second insulating layer 315 is formed above or in direct contact with the etch stop layer 315. The second layer 315 may be formed using the same materials and processes used to form the first insulating layer 305. At step 225, a first patterned mask 320 is formed above or on the insulating layer 315. The first patterned mask 320 includes openings that correspond to the runners or grooves to be formed. In addition, the first patterned mask 320 includes openings that correspond to the openings 327 for a capacitor (hereinafter referred to as the "capacitor openings"). The reticle 390 has a pattern that is translated to the first patterned mask so that the capacitor openings 327 may be formed when openings 325 are formed.

At step 230, capacitor openings 327 and grooves 335 are opened in the second insulating layer 315. The grooves 335 may be formed using conventional etching techniques. During etching, the etch stop layer 310 is used to define the endpoint for this etching process. Subsequently, at step 235, a second patterned mask 330 is formed above or on the first patterned mask 320. The second patterned mask is formed so that the openings in this mask correspond to the via or contact openings (hereinafter "openings") to be formed. Further, the second patterned mask includes openings corresponding to the capacitor openings to be formed. A portion of the second patterned mask may be formed on the walls 350, 351 of the grooves 335. As a result, the walls 350, 351 may not be further etched during the formation of the openings. In contrast, a portion of the second patterned layer may not be formed on the walls of the capacitor openings.

At step 240, the etch stop layer 310 and the first insulating layer 305 are patterned to form openings 325 corresponding to the interconnects between layers to be formed. The capacitor openings 327 are also formed by etching the stop layer 310 and the first insulating layer 305. The openings 325 and capacitor openings 327 may be formed using conventional etching techniques or a combination of techniques to etch through at least the two different layers.

The openings 325 are contained or at least partially contained within boundaries defined by the walls 350, 351 of the grooves 335. Then, at step 245, the remaining portions of the mask layers 320, 330 are stripped using well-known techniques and the partially completed integrated circuit is cleaned at step 247 using conventional processes.

At step 250, a conductive layer 345 is blanket deposited above the second insulating layer 315 and in the openings, grooves, and capacitor openings. Then, the portions of the conductive layer outside the capacitor openings 327 and grooves 335 and on or above the second insulating layer 315 are removed. This may be accomplished using a conventional chemical mechanical polishing process. The conductive layer 345 is a conducting material such as tungsten, aluminum, copper, nickel, polysilicon, or other conducting material suitable for use as a conductor as is known to those skilled in this art.

In an alternative embodiment, one of more layers may be formed prior to the deposition of the conductive layer 345 as described above with regard to the first embodiment and shown in Fig. 15. These one or more layers may be referred to as a liner. In addition, a capping layer as described above with regard to the first embodiment may be provided. Subsequently, the integrated circuit is completed by adding, if necessary, additional metal levels that may including interconnects formed using the process above and conventional processes to complete an integrated circuit.

Although the three layers including the first insulating layer, the etch stop, and the second insulating layer are shown, the number of these layers may be reduced. For example, the capacitor and the dual damascene structure may be formed in one or two insulating layers where the openings for the capacitor and the dual damascene structure are formed at substantially the same time.

Although the invention has been described with reference to exemplary embodiments, it is not limited to those embodiments. Rather, the appended claims should be construed to include other variants and embodiments of the invention that may be made by those skilled in the art without departing from the true spirit and scope of the present invention.

What is Claimed:

1. A method for manufacturing an integrated circuit comprising:

(a) forming an opening in a layer for a dual damascene structure; and

(b) forming at least two openings in the layer for a capacitor.

2. The method of claim 1 wherein steps (a) and (b) occur at substantially the same time.

3. The method of claim 1 wherein step (a) further comprises:

(a1) forming a groove; and

(a2) forming a via.

4. The method of claim 3 wherein steps (a1) and (b) occur at substantially the same time.

5. The method of claim 3 wherein steps (a2) and (b) occur at substantially the same time.

6. The method of claim 1 further comprising:

(c) filling the opening with a conductive material to form a dual damascene structure; and

(d) filling the at least two openings with the conductive material to form the capacitor.

7. The method of claim 6 wherein steps (c) and (d) occur at substantially the same time.

8. The method of claim 1 wherein the layer comprises a plurality of layers.

9. The method of claim 8 wherein the plurality of layers includes at least one etch stop layer.

10. A method of manufacturing an integrated circuit comprising:

(a) forming a plurality of layers;

(b) partially forming a dual damascene structure by forming a first opening in at least one of the plurality of layers; and

(c) partially forming a capacitor by forming second and third openings in at least one of the plurality of layers.

11. The method of claim 10 wherein the first, second, and third openings have substantially the same width.

12. The method of claim 10 wherein the second and third openings have a first width and the first opening has a second width different from the first width.

13. An integrated circuit comprising:

a layer;

a dual damascene structure formed in the layer;

a capacitor formed in the layer, the capacitor having a first conductor and a second conductor formed in the layer.

14. The integrated circuit of claim 13 wherein the layer includes at least two layers.

15. The integrated circuit of claim 13 wherein the first conductor and the second conductor are not formed above or below each other.

16. The integrated circuit of claim 13 wherein:

the layer includes a stop layer; and

the dual damascene structure includes at least a groove and a via where a bottom portion of the groove includes at least a top portion of the stop layer.

17. The integrated circuit of claim 16 wherein the stop layer is formed between the first conductor and the second conductor.

18. The integrated circuit of claim 13 wherein the layer includes a stop layer and the stop layer is formed between the first conductor and the second conductor.

19. The integrated circuit of claim 18 wherein the first conductor and the second conductor contact the stop layer.

20. The integrated circuit of claim 19 wherein the first conductor includes a liner and a conductive material.

21. The integrated circuit of claim 13 wherein the first conductor is a first plate of the capacitor and the second conductor forms the second plate of the capacitor.

22. The integrated circuit of claim 13 further comprising a substrate where the layer is formed on the substrate and the layer is at least not formed between the first conductor and the substrate.

A PROCESS FOR MANUFACTURING AN INTEGRATED CIRCUIT INCLUDING A DUAL-DAMASCENE STRUCTURE AND A CAPACITOR

ABSTRACT

The present invention is directed to a process for forming a dual damascene structure and a capacitor. The process includes forming a stack including insulating layers and a stop layer. The stack is patterned so that the openings used to form the sidewall capacitors may be formed when the vias or grooves of the dual damascene structure is formed. In this way, the process for manufacturing the sidewall capacitors may be integrated with the dual damascene process without adding additional mask or etching steps.

Fig. 1

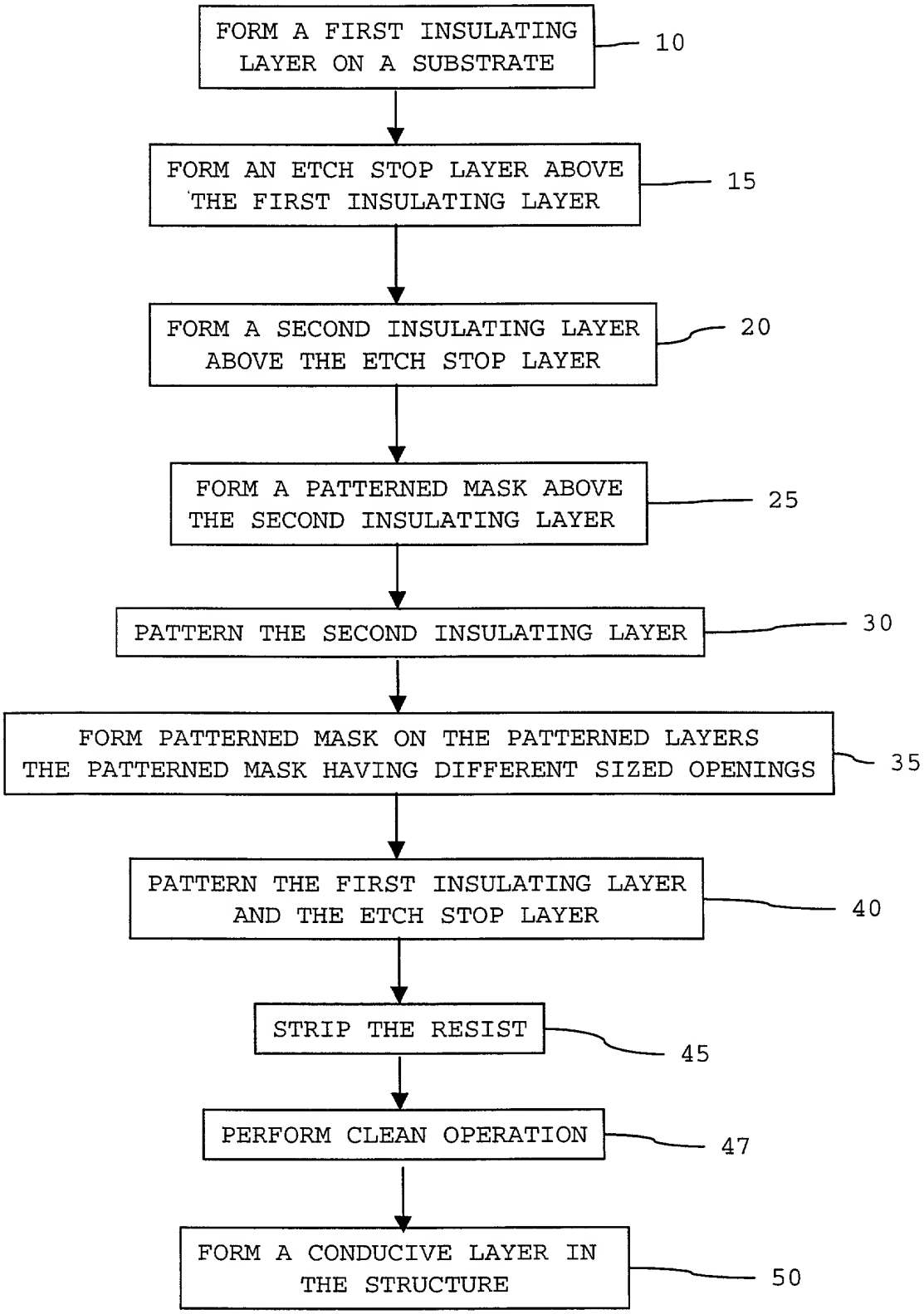

FORM A FIRST INSULATING LAYER ON A SUBSTRATE
10
FORM AN ETCH STOP LAYER ABOVE THE FIRST INSULATING LAYER
15
FORM A SECOND INSULATING LAYER ABOVE THE ETCH STOP LAYER
20
FORM A PATTERNED MASK ABOVE THE SECOND INSULATING LAYER
25
PATTERN THE SECOND INSULATING LAYER
30
FORM PATTERNED MASK ON THE PATTERNED LAYERS THE PATTERNED MASK HAVING DIFFERENT SIZED OPENINGS
35
PATTERN THE FIRST INSULATING LAYER AND THE ETCH STOP LAYER
40
STRIP THE RESIST
45
PERFORM CLEAN OPERATION
47
FORM A CONDUCIVE LAYER IN THE STRUCTURE
50

Fig. 2

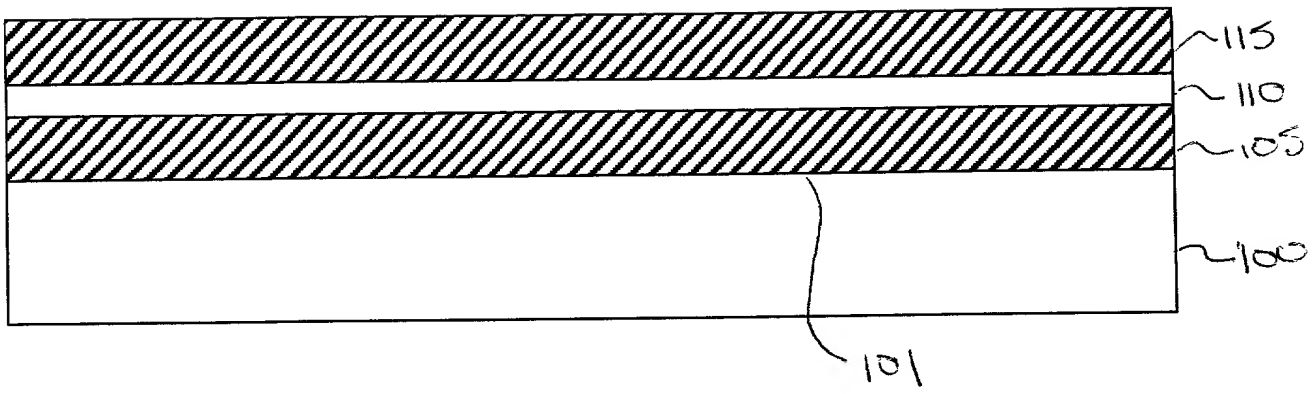


Fig. 3

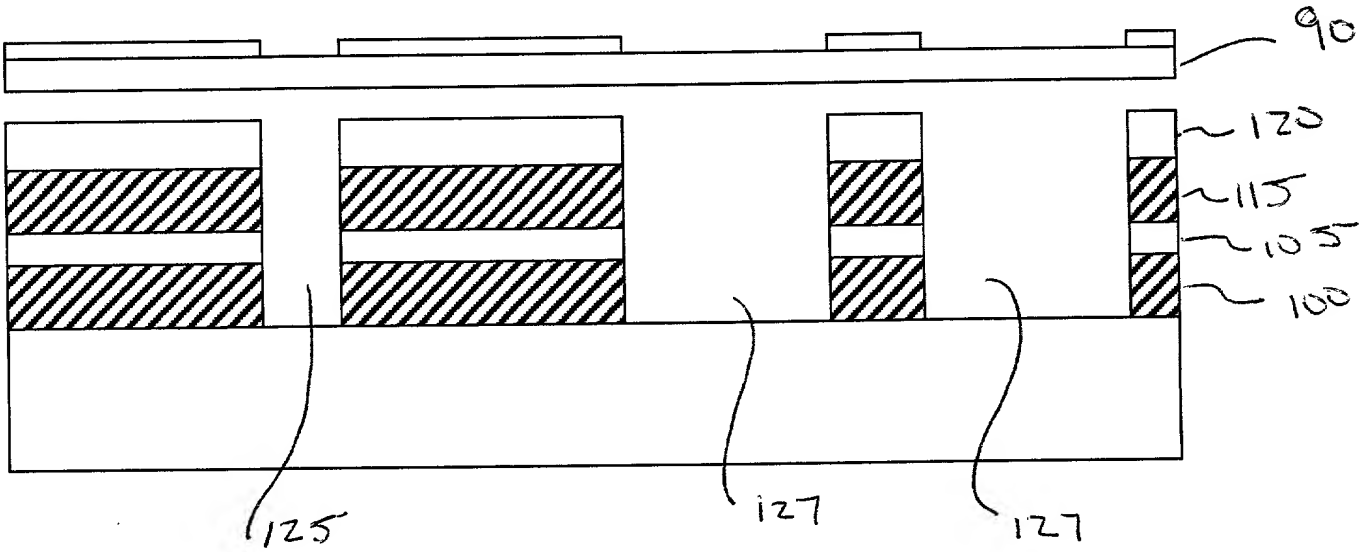


Fig. 4

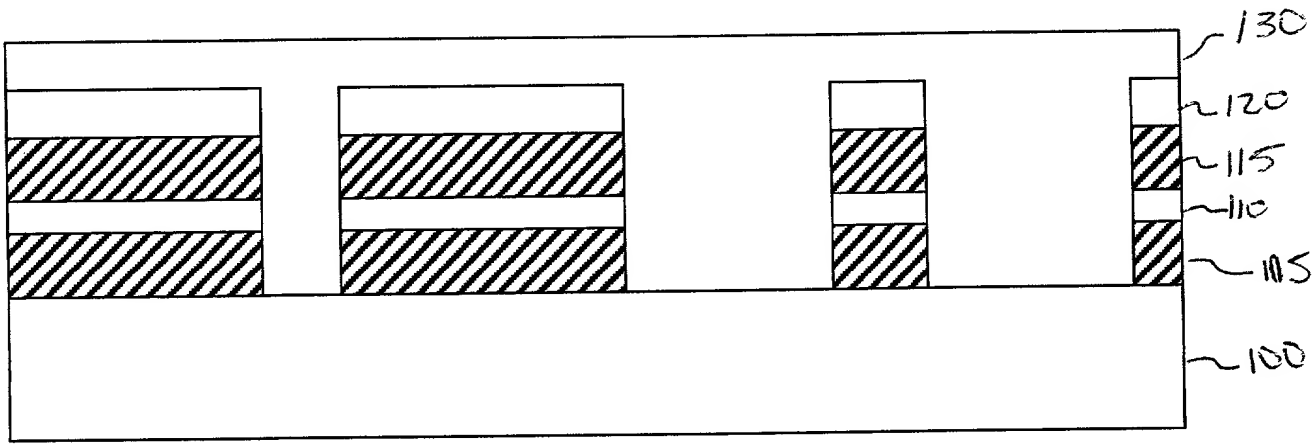


Fig. 5

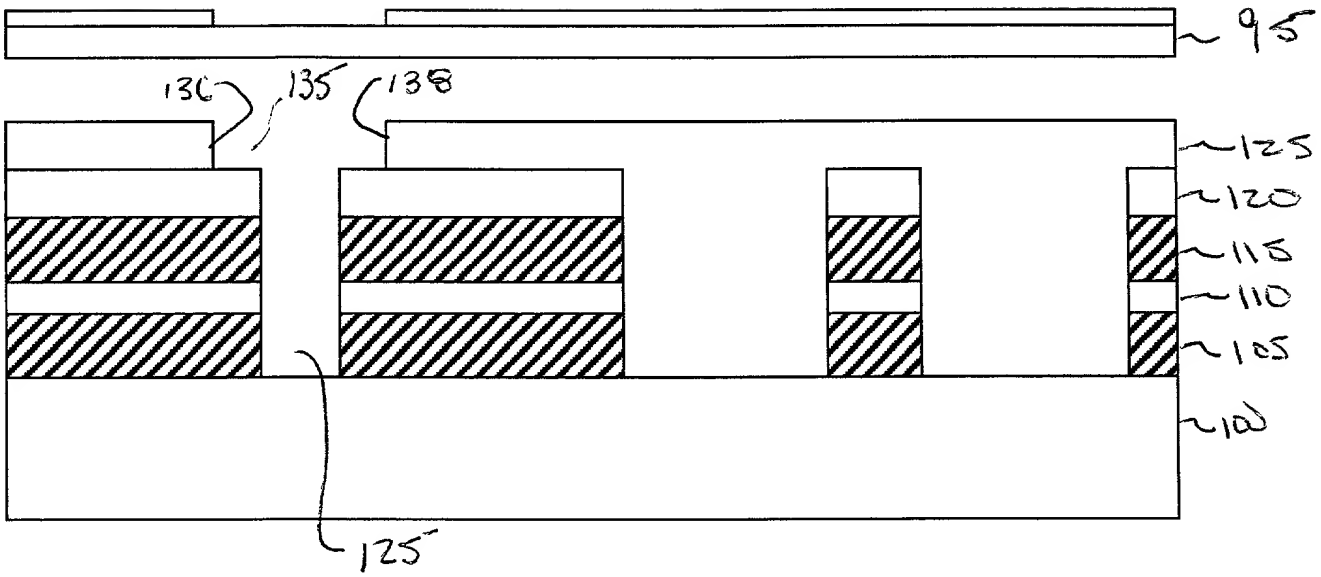


Fig. 6

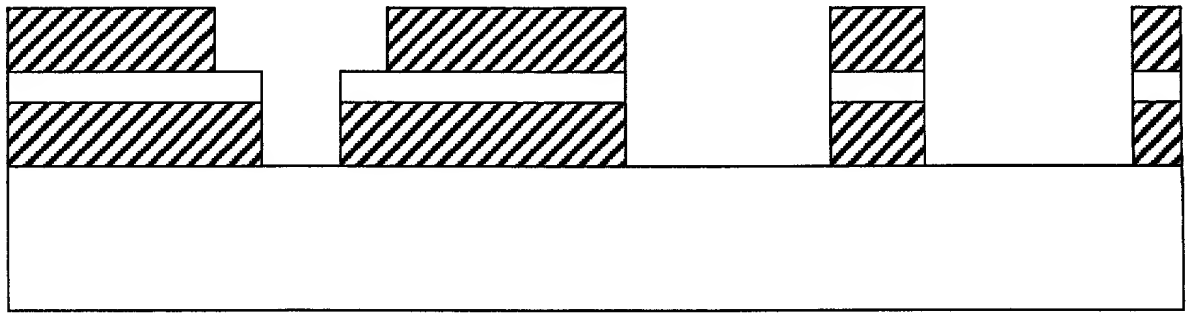


Fig. 7

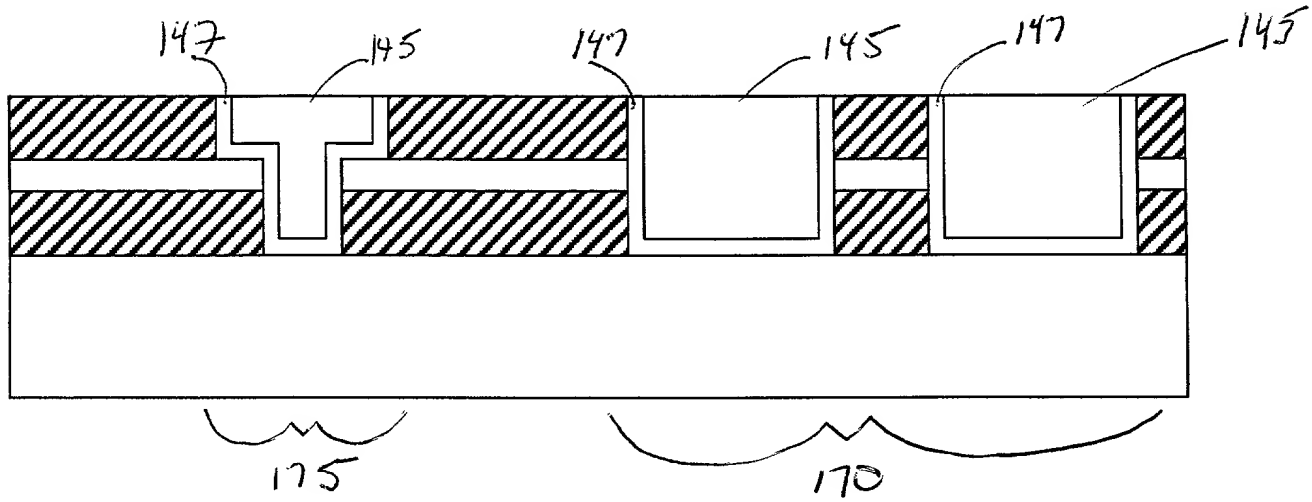


Fig. 8

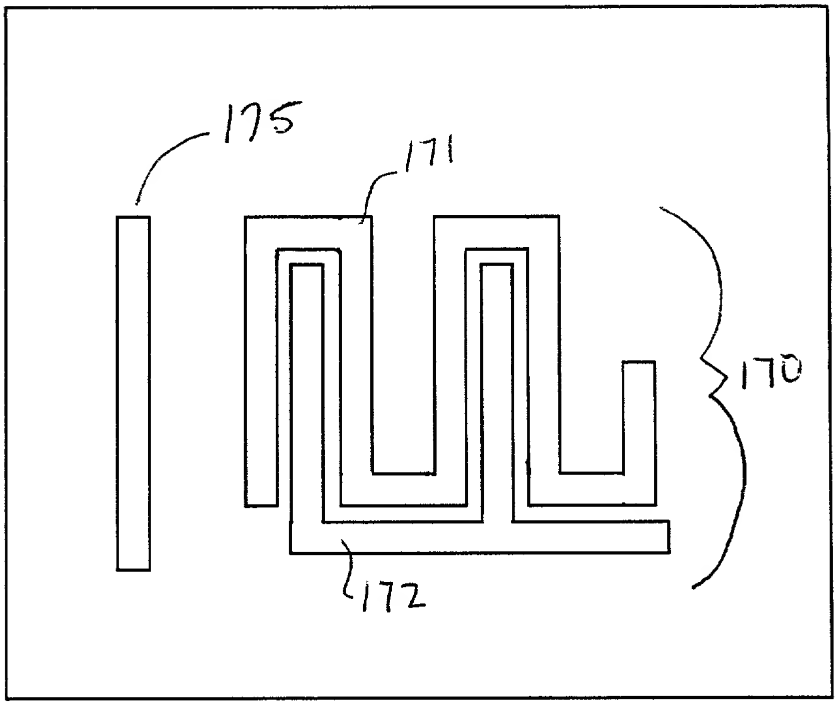
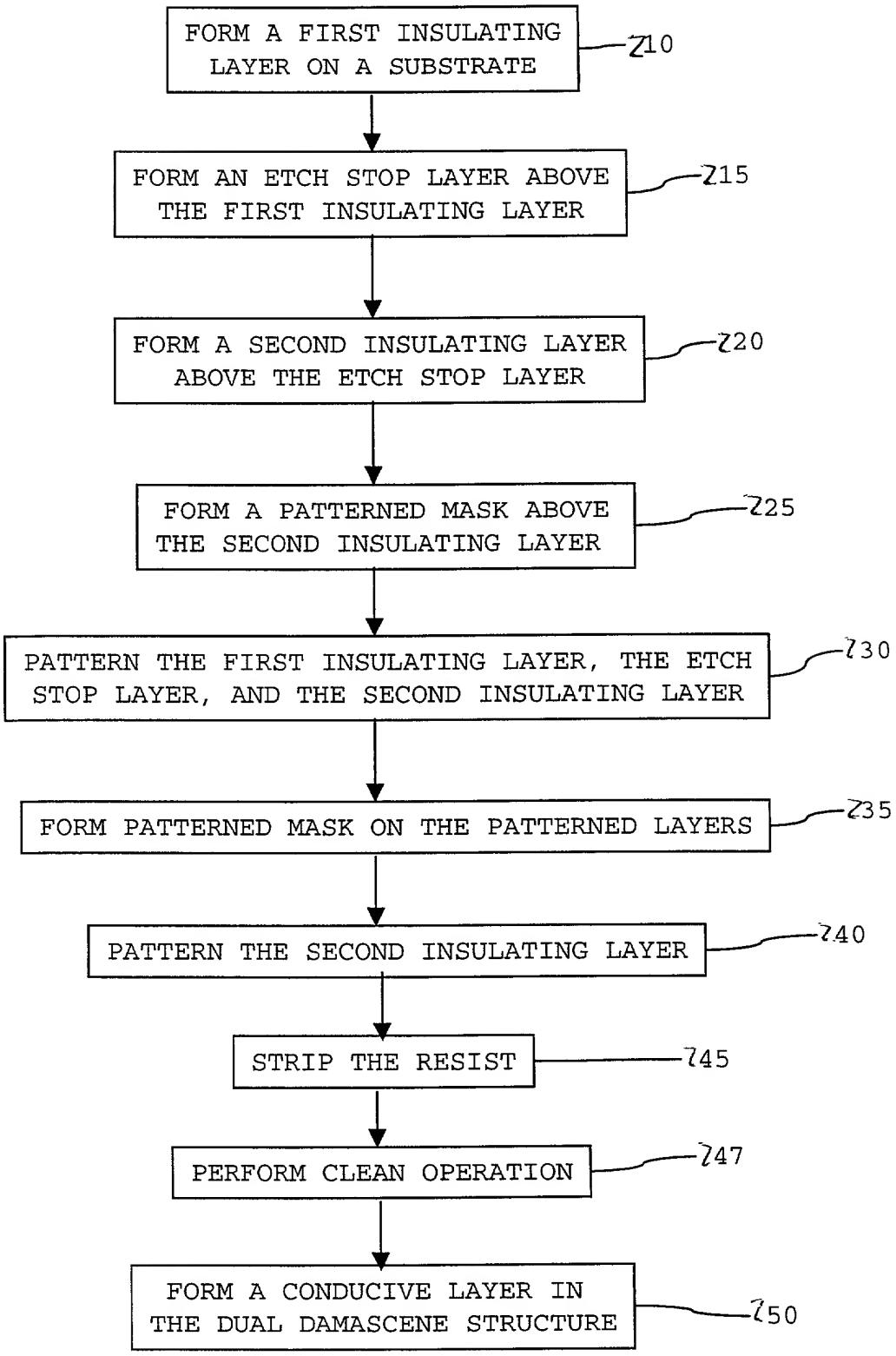


Fig. 9


FORM A FIRST INSULATING LAYER ON A SUBSTRATE
710
FORM AN ETCH STOP LAYER ABOVE THE FIRST INSULATING LAYER
715
FORM A SECOND INSULATING LAYER ABOVE THE ETCH STOP LAYER
720
FORM A PATTERNED MASK ABOVE THE SECOND INSULATING LAYER
725
PATTERN THE FIRST INSULATING LAYER, THE ETCH STOP LAYER, AND THE SECOND INSULATING LAYER
730
FORM PATTERNED MASK ON THE PATTERNED LAYERS
735
PATTERN THE SECOND INSULATING LAYER
740
STRIP THE RESIST
745
PERFORM CLEAN OPERATION
747
FORM A CONDUCIVE LAYER IN THE DUAL DAMASCENE STRUCTURE
750

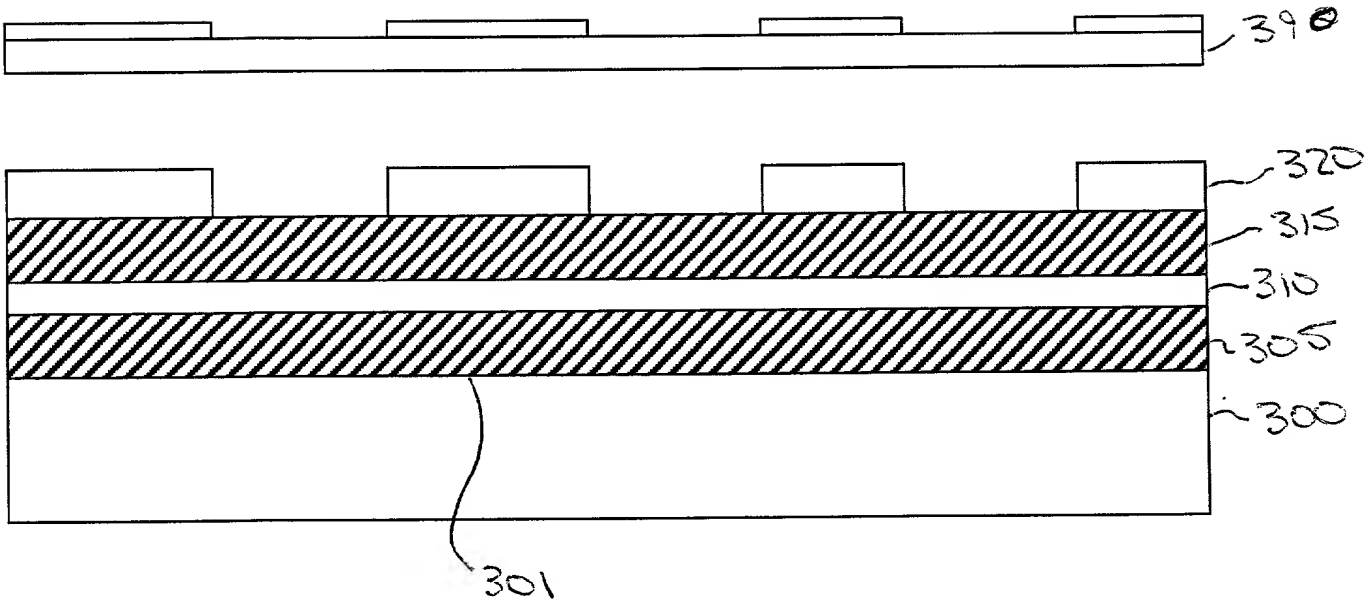


Fig. 10

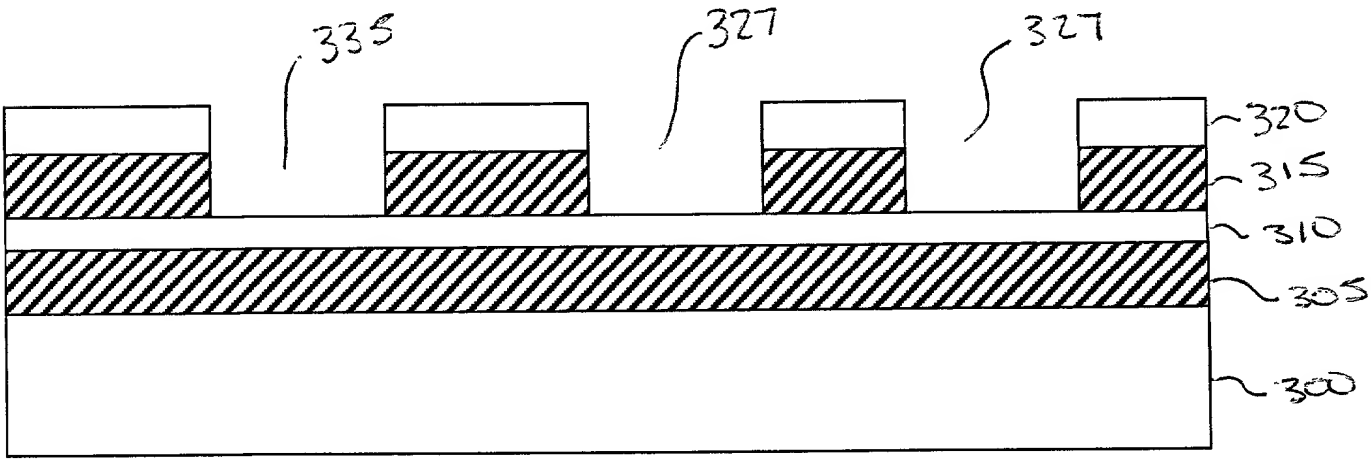


Fig. 11

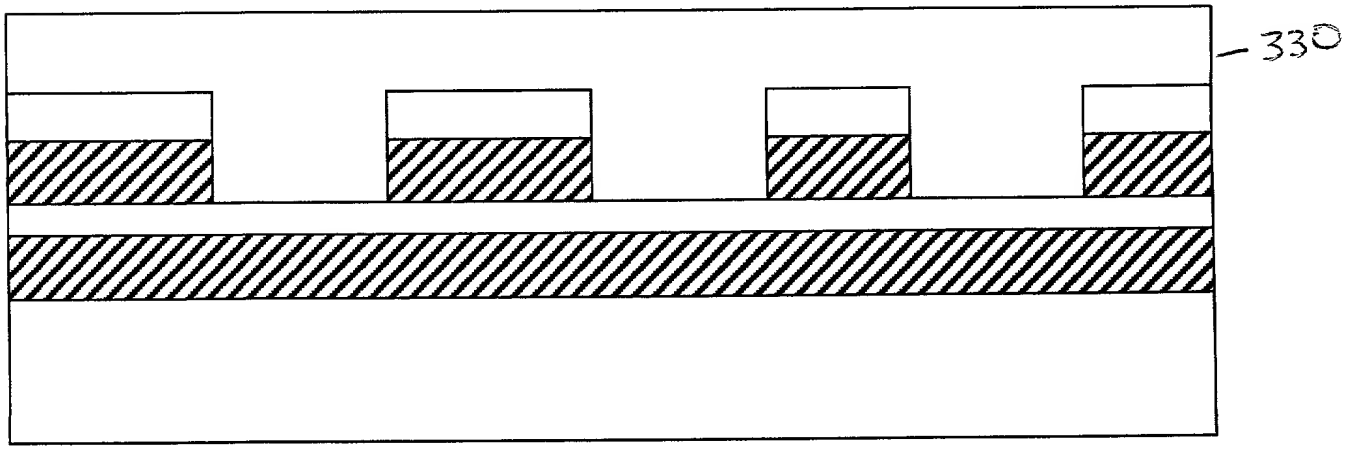


Fig. 12

Fig. 13

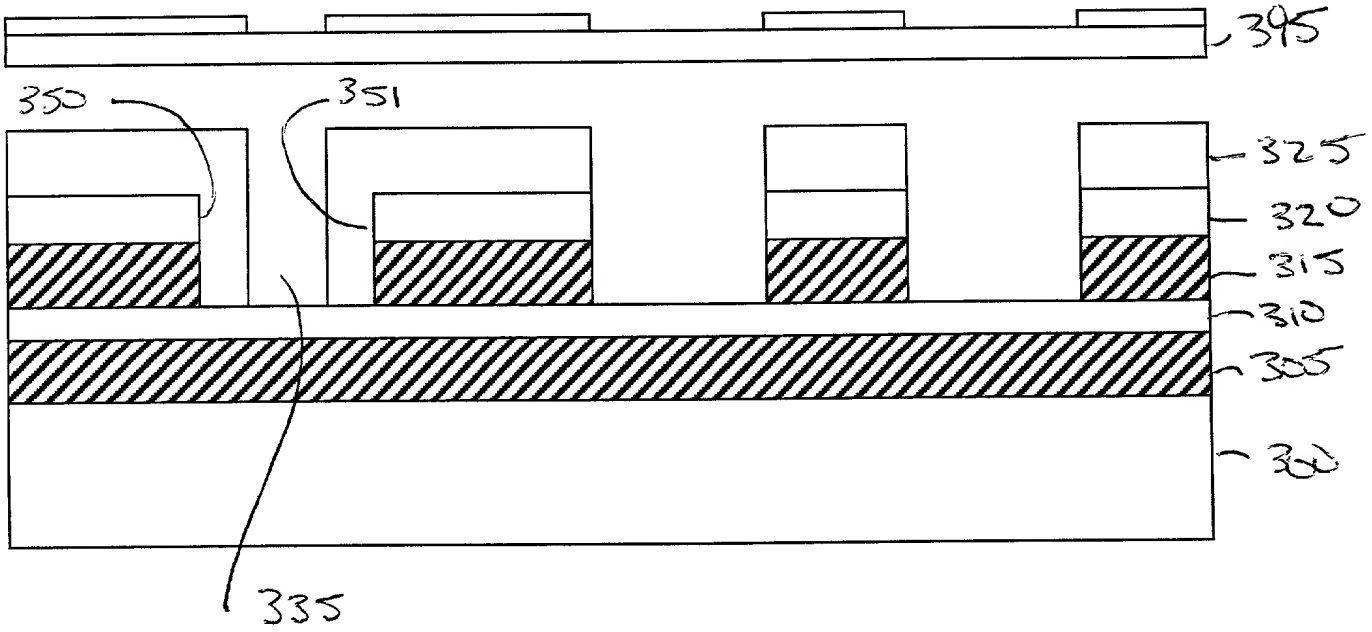


Fig. 14

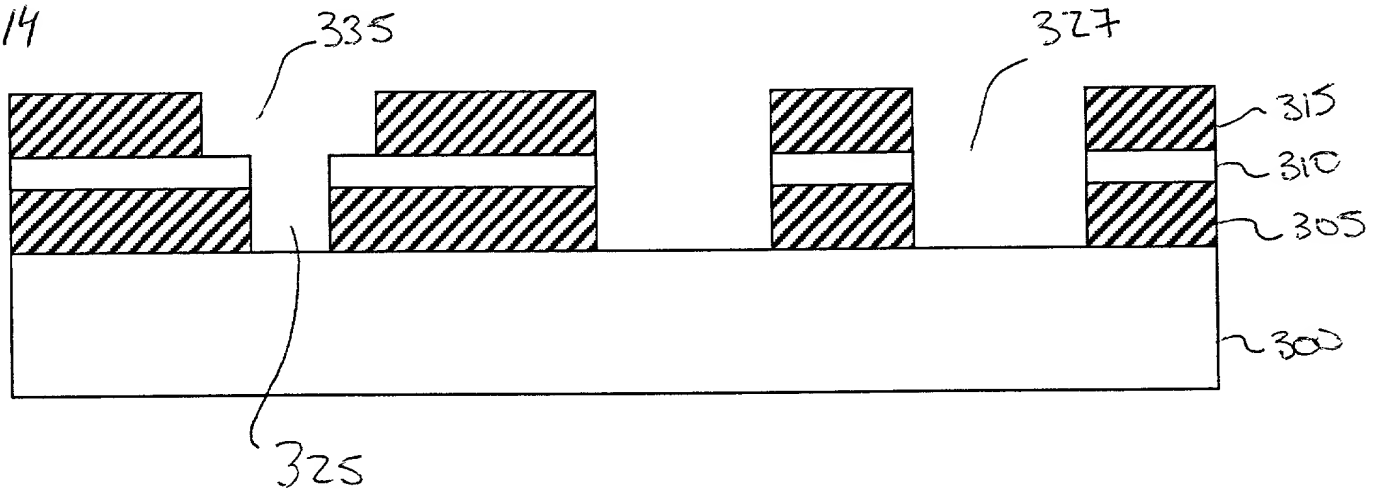
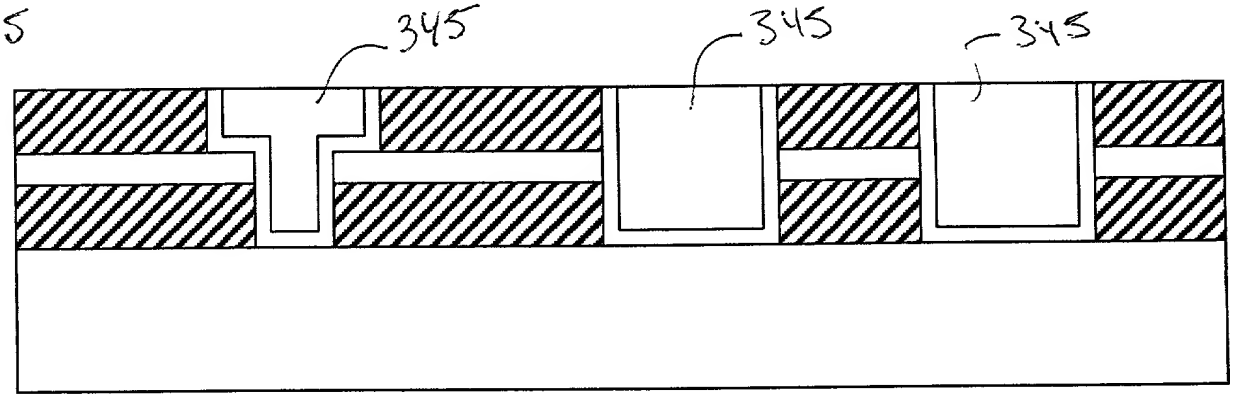


Fig. 15



IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

Declaration and Power of Attorney

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled **A Process For Manufacturing An Integrated Circuit Including A Dual-Damascene Structure And A Capacitor** the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to in this oath or declaration.

I acknowledge the duty to disclose all information known to me which is material to patentability as defined in Title 37, Code of Federal Regulations, 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

None

I hereby claim the benefit under Title 35, United States Code, 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

None

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint the following attorney(s) with full power of substitution and revocation, to prosecute said application, to make alterations and amendments therein, to receive the patent, and to transact all business in the Patent and Trademark Office connected therewith:

Thomas J. Bean	(Reg. No. 44528)
Lester H. Birnbaum	(Reg. No. 25830)
Richard J. Botos	(Reg. No. 32016)
Jeffery J. Brosemer	(Reg. No. 36096)
Kenneth M. Brown	(Reg. No. 37590)
Donald P. Dinella	(Reg. No. 39961)
Martin I. Finston	(Reg. No. 31613)
William S. Francos	(Reg. No. 38456)
Barry H. Freedman	(Reg. No. 26166)
Julio A. Garceran	(Reg. No. 37138)
Jimmy Goo	(Reg. No. 36528)
Anthony Grillo	(Reg. No. 36535)
Stephen M. Gurey	(Reg. No. 27336)
John M. Harman	(Reg. No. 38173)
Matthew J. Hodulik	(Reg. No. 36164)
Michael B. Johannesen	(Reg. No. 35557)
Mark A. Kurisko	(Reg. No. 38944)
Irena Lager	(Reg. No. 39260)
John B. MacIntyre	(Reg. No. 41170)
Christopher N. Malvone	(Reg. No. 34866)
John F. McCabe	(Reg. No. 42854)
Scott W. McLellan	(Reg. No. 30776)
Martin G. Meder	(Reg. No. 34674)
John C. Moran	(Reg. No. 30782)
Michael A. Morra	(Reg. No. 28975)
Gregory J. Murgia	(Reg. No. 41209)
Claude R. Narcisse	(Reg. No. 38979)
Joseph J. Opalach	(Reg. No. 36229)
Neil R. Ormos	(Reg. No. 35309)
Eugen E. Pacher	(Reg. No. 29964)
Jack R. Penrod	(Reg. No. 31864)
Gregory C. Ranieri	(Reg. No. 29695)
Scott J. Rittman	(Reg. No. 39010)
Ferdinand M. Romano	(Reg. No. 32752)
Eugene J. Rosenthal	(Reg. No. 36658)
Bruce S. Schneider	(Reg. No. 27949)
Ronald D. Slusky	(Reg. No. 26585)
David L. Smith	(Reg. No. 30592)
Ozer M. N. Teitelbaum	(Reg. No. 36698)
John P. Veschi	(Reg. No. 39058)
David Volejnicek	(Reg. No. 29355)
Charles L. Warren	(Reg. No. 27407)
Jeffrey M. Weinick	(Reg. No. 36304)
Eli Weiss	(Reg. No. 17765)

Please address all correspondence to the Docket Administrator (Rm. 3C-512), Lucent Technologies Inc., 600 Mountain Avenue, P. O. Box 636, Murray Hill, New Jersey 07974-0636. Telephone calls should be made to Anthony Grillo by dialing 610-712-3766.

Full name of sole inventor: Sailesh Chittipeddi

Inventor's signature  Date 6/16/00

Residence: Allentown, Lehigh County, Pennsylvania

Citizenship: United States of America

Post Office Address: 308 Lenape Trail
Allentown, Pennsylvania, 18104